AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS

1. (Previously Presented) An apparatus comprising:

a first wafer having a first interlayer dielectric layer and a first plurality of copper structures of first substantially uniform heights with each difference between any two of the first substantially uniform heights being 5 nm or less, disposed on the first interlayer dielectric layer; and

a second wafer having a second interlayer dielectric layer and a second plurality of copper structures of second substantially uniform heights with each difference between any two of the second substantially uniform heights being 5nm or less, disposed on the second interlayer dielectric layer, the second wafer being stacked on the first wafer, with at least some of the first and second plurality of copper structures being substantially aligned and bonded to each other.

2. (Original) The apparatus of claim 1, wherein at least a selected one of the first and second substantially uniform heights is in a range of 100-300nm.

3. (Original) The apparatus of claim 2, wherein both the first and second substantially uniform heights are in the range of 100-300nm.

4. (Withdrawn) A method comprising:

providing a first wafer comprising first copper structures encased in a first interlayer dielectric layer; and

wet etching the first wafer to expose the first copper structures with the first copper structures having first substantially uniform heights, where each difference between any two of the first substantially uniform heights is 5 nm or less.

5. (Withdrawn) The method of claim 4, wherein the etching comprises etching the first wafer using a diluted organic hydrofluoric acid, assisted by a super critical CO_2 to remove part of the interlayer dielectric layer.

6. (Withdrawn) The method of claim 5, further comprises rinsing the first wafer with deionized water.

7. (Withdrawn) The method of claim 4, wherein the etching comprises etching the first wafer using a diluted hydrofluoric acid to selectively remove part of the interlayer dielectric layer.

8. (Withdrawn) The method of claim 4, wherein the etching comprises etching the first wafer using an ethylene glycol based solution and a diluted hydrofluoric acid to remove part of the interlayer dielectric layer.

9. (Withdrawn) The method of claim 4, wherein the etching comprises etching the first wafer using a buffered oxide etch reactant to remove parts of the interlayer dielectric layer.

10. (Withdrawn) The method of claim 4, wherein the etching comprises etching the wafer using a buffered oxide etch reactant and a diluted hydrofluoric acid to remove part of the interlayer dielectric layer.

11. (Withdrawn) The method of claim 4, wherein the etching comprises etching the wafer using a buffered oxide etch reactant, an ethylene glycol based solution and a diluted hydrofluoric acid to remove part of the interlayer dielectric layer.

12. (Withdrawn) The method of claim 4, wherein the method further comprises performing a reactive pre-cleans using hydrogen-based plasma to remove residues on a surface of the copper structures.

13. (Withdrawn) The method of claim 4, wherein the method further comprises

providing a second wafer comprising second copper structures encased in a second interlayer dielectric layer; and

wet etching the second wafer to expose the second copper structures with the second copper structures having second substantially uniform heights, where each difference between any two of the second substantially uniform heights is 5 nm or less.

14. (Withdrawn) The method of claim 13, wherein the method further comprises

aligning the first and second wafers; and

bonding at least some of the first copper structures to some of the second copper structures to bond and stack the first wafer on the second wafer.

15. (Previously Presented) A system comprising:

a semiconductor package having

a first die having a first interlayer dielectric layer and a first plurality of copper structures of first substantially uniform heights disposed on the first interlayer dielectric layer, where each difference between any two of the first substantially uniform heights is 5 nm or less; and

a second die having a second interlayer dielectric layer and a second plurality of copper structures of second substantially uniform heights disposed on the second interlayer dielectric layer, where each difference between any two of the second substantially uniform heights is 5 nm or less, the second die being stacked on the first die, with at least some of the first and second plurality of copper structures being substantially aligned and bonded to each other;

a bus coupled to the semiconductor package; and

a networking interface component coupled to the bus.

16. (Original) The system of claim 15, wherein at least a selected one of the first and second substantially uniform heights of the semiconductor package is in a range of 100-300nm.

17. (Original) The system of claim 16, wherein both of the first and second substantially uniform heights of the semiconductor package is in the range of 100-300nm.

18. (Original) The system of claim 15, wherein the system is a selected one of a digital versatile disk player and a set-top box.

19. (Previously Presented) An apparatus comprising:

a first wafer having a first interlayer dielectric layer and a first plurality of electrically conductive structures of first substantially uniform heights with each difference between any two of the first substantially uniform heights being in a range of 1nm to 5nm, disposed on the first interlayer dielectric layer; and

a second wafer having a second interlayer dielectric layer and a second plurality of electrically conductive structures of second substantially uniform heights with each difference between any two of the first substantially uniform heights being in a range of 1nm to 5nm, disposed on the second interlayer dielectric layer, the second wafer being stacked on the first wafer, with at least some of the first and second plurality of electrically conductive structures being substantially aligned and bonded to each other.

20. (Previously Presented) The apparatus of claim 19, wherein at least a selected one of the first and second substantially uniform heights is in a range of 100nm to 300nm.

21. (Previously Presented) The apparatus of claim 19, wherein both the first and second substantially uniform heights are in the range of 100nm to 300nm.

22. (Previously Presented) A system comprising:

a semiconductor package having

a first die having a first interlayer dielectric layer and a first plurality of electrically conductive structures of first substantially uniform heights with each difference between any two of the first substantially uniform heights being in a range of 1nm to 5nm; and

a second die having a second interlayer dielectric layer and a second plurality of electrically conductive structures of second substantially uniform heights with each difference between any two of the second substantially uniform heights being in a range of 1nm to 5nm, the second die being stacked on the first die, with at least some of the first and second plurality of copper structures being substantially aligned and bonded to each other;

a bus coupled to the semiconductor package; and

a networking interface component coupled to the bus.

23. (Previously Presented) The system of claim 22, wherein at least a selected one of the first and second substantially uniform heights of the semiconductor package is in a range of 100nm to 300nm.

24. (Previously Presented) The system of claim 23, wherein both of the first and second substantially uniform heights of the semiconductor package is in the range of 100nm to 300nm.

25. (Previously Presented) The system of claim 22, wherein the system is a selected one of a digital versatile disk player and a set-top box.